REMARKS

Claims 1-12 are pending in the application. Claims 1-2, 4, 6 and 8-12 are rejected. Dependent claims 3, 5 and 7 are objected to as being dependent on a rejected base claim but would be allowable if rewritten into independent form.

Information Disclosure Statement

Applicants note that the Office Action did not include any indication that the references cited in an Information Disclosure Statement (IDS) submitted on April 19, 2004 were considered. Inasmuch as the US PTO has confirmed receipt of the IDS on April 22, 2004, Applicants believe this omission is due to mere oversight. Nevertheless, as a precaution and as a convenience to the Examiner, Applicants include herewith a copy of the form PTO-1449 that accompanied the IDS and request that that the Examiner make the cited references of record in this application.

Amendments to Specification

Applicants amend the specification as shown above to correct a spelling error.

Rejection of Claims

Claims 1-2, 4, 6 and 8-10 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. patent 6,031,386 (referred to as "Cole") in view of Acuna et al., "Simulation Techniques for Mixed Analog/Digital Circuits," IEEE J. of Solid-State Circuits, April 1990, vol. 25, no. 2, pp. 353-363 (referred to as "Acuna").

Referring to claim 1, the Office Action indicates Cole teaches all that is claimed except that the numerical modeling disclosed therein is a logic simulation as opposed to a transition simulation. Applicants respectfully disagree and traverse the rejection of claim 1 because Cole and Acuna, either alone or in combination, do not disclose or suggest all limitations of claim 1. Applicants refer more particularly to the last step of method claim 1, which they believe can be easily seen is not taught by the cited references.

Cole teaches methods for testing an integrated circuit (IC) that either measures the transient component of the IC operating voltage (see col. 3, lns. 33-39) or the time delay of the transient component of the operating voltage (col. 3, lns. 47-52). Reference values that may be used to determine if a measured component is out of bounds, thereby indicating a failure exists in the IC, may be obtained by measuring known good ICs or by numerical modeling (col. 3, lns. 42-45 and 59-62). Acuna teaches methods for circuit simulation, which can be used for the numerical modeling mentioned in Cole.

Contrary to what is taught in these references, the method of claim 1 is not directed toward testing semiconductor ICs *per se*. Claim 1 recites steps of a method for generating a list of faults in a semiconductor IC that are capable of being detected by transient power supply testing. The method of claim 1 does not actually test an IC but instead produces a list of faults that may be used to design a set of test patterns for more efficient testing.

Neither Cole nor Acuna disclose or suggest anything that is pertinent to determining which faults are capable of being detected by transient power supply current testing. Cole tacitly admits its disclosed method of testing, as well as other known methods of testing, are incapable of detecting all kinds of faults. In particular, Cole states the following:

> Pinpointing of different types of defects and failure mechanisms in an IC generally requires the use of different analytical methods, since each analytical method has certain advantages and disadvantages (col. 1, lns 26-29).

Although Cole indicates not all types of faults can be detected by a given method of testing, Cole does not teach anything that allows a person of ordinary skill in the art to determine which faults are capable of being detected by its disclosed methods of testing or by any other methods of testing.

Furthermore, neither Cole nor Acuna disclose or suggest the second step recited in claim 1 in which two or more test patterns are applied to calculate logic value sequences in each signal line of an IC.

Similar reasons apply to claim 10. Claims 2-9 are dependent on claim 1 and add further limitations.

Claims 11-12 are rejected under 35 U.S.C. § 103 as being unpatentable over Cole in view of Carmichael et al., "Simulation as an aid to power supply diagnostics," Conf. Record of AUTOTESTCON '95, Atlanta, Aug. 8-10, 1995, pp. 556-56- (referred to as "Carmichael").

Referring to claim 11, the Office Action indicates Cole teaches all that is claimed except for specifically mentioned limitations that pertain to inserting an assumed fault in a semiconductor IC and deciding whether the assumed fault is detectable.

As explained above, Cole does not disclose or suggest how to determine which faults are detectable by transient power supply testing. This alone is sufficient to traverse the rejection of claim 11.

In addition, as stated in the Office Action, Cole does not disclose or suggest inserting an assumed fault into a circuit simulation and determining whether the assumed fault is capable of being detected; however, the Office Action alleges this missing teaching is provided by Carmichael. Applicants respectfully disagree.

Carmichael discusses research in which engineers simulated operation of a power supply circuit with a numerical model and used this model as an aid to determine manually how several assumed faults affected circuit operation. There is no teaching or suggestion for any technique that determines whether a particular fault can be detected by transient power supply current testing. Indeed, this type of testing is not even mentioned.

In view of these omissions, Applicants respectfully submit claim 11 is patentable over the cited combination of references. Analogous reasons apply to claim 12.

CONCLUSION

Applicants amend the specification as shown above, request that the references disclosed in a previously submitted Information Disclosure Statement be made of record in this application, and request reconsideration of the claims in view of the discussion set forth above.

Respectfully submitted,

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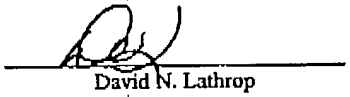
Certificate of Transmission

I certify that this Response to Office Action and any following materials are being transmitted by facsimile on August 3, 2004 to the U.S. Patent and Trademark Office at telephone number (703) 872-9306.



David N. Lathrop

Enc. Copy of PTO-1449 that accompanied previously submitted IDS

SHEET 1 OF 1

Form PTO-1449 — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

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APPLICANT: Masahiro Ishida, et al.	
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U.S. PATENT DOCUMENTS

*Exam. Initial		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

*Exam. Initial		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	EP	0878761	11-18-98	European Patent Office				

OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Pages, etc.*)

EXAMINER: | DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.